French Contribution To The Construction Of SKA-MID

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Outline

- Receiver overview
- First Design
- New Design
- Development plan
Receiver overview

- 5 SKA-MID Bands with two polarization signals
  - B1: from 0.35 GHz to 1.05 GHz sampled at 4 GSps
  - B2: from 0.95 GHz to 1.76 GHz sampled at 4 GSps
  - B3: from 1.65 GHz to 3.05 GHz sampled at 3.2 GSPs
  - B4: from 2.8 GHz to 5.2 GHz sampled at 16 GSps
  - B5a: from 4.6 GHz to 8.5 GHz sampled at 9 GSps
  - B5b: from 8.3 GHz to 15.4 GHz sampled at 16 GSps
Receiver overview
Development Phase

3-bit at 26 GSps
Eval. Board
Prototype Board
Last time to buy

4-bit at 16 GSps
Eval. Board
Prototype Board
ENOB < 3 bits

6-bit at 32 GSps
Eval. Board
Prototype Board in progress

ECP: E5a & E5b

PDR: July 2017

ECP: Talon board

SKAO: May 2022

DDR: July 2023

CDR: end of 2023
First Design

- Based on 4-bit ADC at 16 GSps
  - Two ADC boards (B5a at 9 GSps and B5b at 16 GSps)
  - Two RF boards with two outputs (one per band)
  - Two sampling clocks (9 GHz and 16 GHz)
First Design

- Our design is based on the NRC design
  - A PSU enclosure
  - A main enclosure composed of two cavities
    - RF cavity
    - Digital cavity with two levels of EMI shielding
First Design

- Examples of realization

3.96 GHz

15.84 GHz

8.91 GHz
# First Design: Results

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| **RXS45.ODL** | 4 RF enclosures | 3 boards | Measurements | Measurements | - RFI on site: < 3 bits  
- Additional bit needed for slope correction  
- Adsantec: production? |
| **RXS45.PWR** | 1 PSU enclosure | Simulation | Analysis | Analysis | - Power loss too important |
| **RXS45**     | 1 main enclosure | B5b | Analysis | Analysis | - not ready for an end-to-end test |

- Meeting at LAB with SKAO in May 2022  
  ⇒ New design with higher resolution ADC.
New Design

- 6-bit ADC at 32 GSps: first Nyquist zone includes B5a & B5b:
New Design

- **Adsantec solution** ⇒ **Micram solution**
  - Two ADC boards (B5a at 9 GSps and B5b at 16 GSps)
  - Two RF boards with two outputs (one per band)
  - Two sampling clocks (9 GHz and 16 GHz)
New Design

- Adsantec solution $\Rightarrow$ Micram solution
  - Only one ADC board
  - One output for RF board
  - One clock at 16 GHz
New Design

- 5 SKA-MID Bands with two polarization signals
  - B1: from 0.35 GHz to 1.05 GHz sampled at 4 GSPs
  - B2: from 0.95 GHz to 1.76 GHz sampled at 4 GSPs
  - B3: from 1.65 GHz to 3.05 GHz sampled at 3.2 GSPs
  - B4: from 2.8 GHz to 5.2 GHz sampled at 32 GSPs
  - B5a: from 4.6 GHz to 8.5 GHz sampled at 32 GSPs
  - B5b: from 8.3 GHz to 15.4 GHz sampled at 32 GSPs
Development Plan

- Design changes
  - Only one ADC board with two ADCs at 32 GSps: first Nyquist zone includes B5a and B5b
  - 48 outputs at 8 Gbps instead of 16 outputs at 16 Gbps $\Rightarrow 4 \times \text{Tx12}$ (ADC outputs) and B04 (control and monitoring data)
  - RF chain very similar to Adsantec solution
  - Clock synthesizer board is simpler (only frequency multiplication by 4)

  - Thermal analysis to be done (13 W each)
  - Several shielding layers to be implemented
  - Mechanical enclosure to be redesigned

  - RXPU: Additional FPGA board to be designed for the B5 receiver interfacing with the Talon board (FPGA board developed by NRC)
  - For CDR: use a Talon board (to be discussed with SKAO)
Development Plan

- Goal is to pass the Critical Design Review (CDR) before end of 2023
- In one year, a lot of activities to be done: design, fabrication, test, document submission for reviews
- Two prototypes tested on site
- Detailed design review in June/July 2023: end-to-end test results in lab environment with EMC qualification (electromagnetic reverberation chamber at Airbus in Toulouse)
- Mechanical design based on NRC design with some changes from Swedish team
- Support from FEDD for industrialization
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